

Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

## U.S. UTILITY Patent Application

**O.I.P.E.**

**PATENT DATE**

**SCANNED**

## Q.A

APPLICATION NO. 09/765958	CONT/PRIOR D	CLASS 714 <del>202</del>	SUBCLASS 729	ART UNIT <del>2057</del> 2123	EXAMINER Dooley
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## APPLICANTS

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2133

# FILE

### Hierarchical test circuit structure for chips with multiple circuit blocks

PTO-2040  
12/89

# ISSUING CLASSIFICATION

ORIGINAL					CROSS REFERENCE(S)								
CLASS		SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION													

☐ Continued on Issue Slip Inside File Jacket

<input checked="" type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>		<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b> _____ _____	
<input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. <u>6,163,504</u>	_____ (Primary Examiner) (Date)		<b>ISSUE FEE</b> Amount Due _____ Date Paid _____	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)		<b>ISSUE BATCH NUMBER</b> _____	
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